Experiment 8

Synthesis Using Programmable Logic Devices

1. Purpose
   To use Altera Max Plus II to synthesize circuits and to program a logic device.

2. Prelab
   Carefully read the experiment discussion and procedure. Reprint the circuit diagrams and simulation timing diagrams in Sections 6.1 and 6.9.

3. Reference
   *Max Plus II Getting Started* by Altera Co.

4. Discussion

4.1. Programmable Logic Device

Before the advent of programmable logic, custom logic circuits were built using standard off-the-shelf components (e.g. TTL chips), or expensive application-specific (custom) integrated circuits (ASIC). PLDs are normally organized as arrays of logic cells connected by interconnect matrix. Each logic cell can be viewed as a standard component that can be independently “programmed” to perform a small set of functions. The individual cells are connected by interconnect matrices that consist of wires and programmable switches. Complex designs can be created by combining these basic cells to create the desired circuit. A design is implemented by specifying the logic function for each cell and the connection of the interconnect matrix. All these are done by short-circuiting selected interconnection points and switches, which is known as “programming the device”. Next lecture will provide more detailed information.

4.2. Revisit of Altera *Max Plus II*

We have used Altera Max Plus II to do schematic entry and simulation for TTL based circuits in the previous experiments. Max Plus II can also perform synthesis and device programming. Synthesis is process that converts the original design entry to a circuit consisting of basic logic cells of a programmable device. It is known as compiling in Max Plus II. During the synthesis, the “fuse pattern” is also determined and stored in a file. Device programming is the process that physically “burns” the fuses of a programmable device according to a given file.

The typical design flow of PLD circuits is shown below:
We first create the design entry, and synthesize the design and then perform simulation to verify its operation. If the response is not correct, we need to revise the design and repeat the process. After the circuit is verified, we can then program the PLD chip, connect the input signals and do physical testing. When a circuit is implemented by PLD, we essentially create a customized chip. The only wiring required is the power and ground of the PLD device and testing signals.

5. Components

Altera EPM7128S and 74LS163. Unlike TTL, EPM7128S is more expensive and the department only has a limited quantity. Handle the chip carefully and pay particular attention to the chip orientation and circuit wiring. Damaging the chip or device programmer will severely lower your grade.

6. Procedures

6.1. Create a project file test1.gdf

(a). Open the graphic file test1.gdf of experiment 2 and set it as the project file. Recreate it if necessary.

![Diagram]

6.2. Compile (synthesize) the project test1.gdf to EPM7128

(a). There are a wide variety of PLD devices from Altera and the intended device has to be specified before compiling (we let the software choose a device automatically in previous experiments). The device used in our lab is EPM7128SLC84.

(b). Select Max+plus II then Compiler and the compiler window appears.

(c). Select Assign then Devices...

(d). In dialog window, select MAX7000S in Device Family entry and then select EPM7128SLC84-6 in Devices entry. Click OK.

(e). Compile the project as before.

(f). Note that inside the Compiler window, there is an rpt file under Fitter and a pof file under Assembler. They are report file and “fuse map” file respectively. They can be found as test1.rpt and test1.pof in project directory.

(g). Create a waveform file and then simulate the design to verify its operation.
6.3. Wire the adaptor board

(a). EPM7128SLC84 is in 84-pin PLCC package. A special adaptor board is needed for the CADET or breadboard, as shown below.

(b). Put the adaptor board into the breadboard. Make sure the connection is tight. You can leave the adapter board on CADET for the experiments of the remaining semester.

(c). The pin-out diagram is of 7128SLC84 is shown below. The pins labeled with I/O will be assigned during compiling for input and output signals. The pins labeled with VCC (for both VCCIO and VCINT) and GND are power and ground respectively.
(d). Connect the VCC and GND pins according to the diagram. Make sure that wires are short and connection is tight. Use the proper color. You will keep the wiring for the remaining semester.

(e). Turn on the power of CADET and use the logic probe to check all VCC and GND pins of the adaptor board. Make sure that all of them are properly connected. Turn off the power.

(f). Orientation of 7128SLC84 is done by the notch in the top left corner, as shown in previous diagram. Identify the notch of 7128SLC84 and the notch of the socket of the adaptor board. Insert 7128S into the socket according to the orientation.

6.4. Wire the download cable socket

(a). 7128SLC84 is programmed via 4 special-purpose pins: TDI (pin 14), TMS (pin 23), TCK (pin 62) and TDO (pin 71), as shown in the previous pin-out diagram.

(b). The CADET breadboard can be connected to the device programmer (named as MasterBlaster by Altera) by a special cable. One end of the cable is a 14-pin socket shown below (left two diagrams).

(c). Only 8 pins of the 14-pin socket are used. The pin-assignment of the 14-pin socket is shown above (right diagram). Note that the red stripe of the cable is connected to the pin 1 of the socket. Pins 4, 6, 7, 8, 9 and 11 are not used.

(d). Connect VCC and GND to power and ground respectively. Connect TDI, TMS, TCK and TDO to the corresponding pins of the adaptor board. You will keep this part of wiring for the remaining semester, too.

(e). Double-check the wiring.
6.5. Connect the device programmer (MasterBlaster)
(a). Make sure that the CADET’s power is turned off.
(b). The MasterBlaster is shown below.
(c). Connect one end of the white cable to a USB port of PC. The USB plug is directional. If you cannot insert it into PC, turn it other way. Don’t push it too hard.
(d). Connect the other end of the white cable to MasterBlaster.
(e). Connect one end of the gray ribbon cable to MasterBlaster. Put the socket of the other end to the stripes wired in section 6.4.

6.6. Program the 7128S device
(a). Turn on the power of CADET.
(b). Start Max Plus II, if you haven’t done so.
(c). Select Max+plus II then Programmer and the programmer window appears.
(d). Select Option then Hardware Setup... and a dialog window appears.
(e). If the MasterBlaster is not appeared as the default programmer, select MasterBlaster from Hardware Type: entry and then OK.
(f). Select JTAG and then turn on Multi-Device JTAG Chain.
(g). Select JTAG then Multi-Device JTAG Setup and a dialog window appears.
(h). Select Select Programming File, move to the directory that contains test1.pof and then choose test1.pof.
(i). Click Add and test1.pof should appear in the middle box. Click OK to close the window.
(j). If there are other pre-existing .pof files in the middle box, remove them by highlight them and clicking Delete.
(k). Select EPM7128S from the Device Name list box I
(l). Return to Programmer Window and click Program button. The bar on bottom should gradually reach 100% mark. Close the window when it is done.

(m). Turn off the power of CADET.

(n). Remove the download cable.

6.7. Check the report file for pin assignment

(a). During compiling, MAX Plus II automatically chooses physical I/O pins for the input and output stubs of the design files. This information is recorded in report file (.rpt). Note that the pin assignment may change after re-compiling even the circuit remains the same. If you want to physically wire the chip, it is important to check the report file after every compiling.

(b). The easiest way to open the report file is to open the Hierarchy Display window and double click rpt icon under the project.

(c). There is lots of information in report file. The pin assignment can be found in “Device-Specific Information” section. If you want to print the pin assignment, highlight this part and print the selected area, or you will print the entire report which is rather large.

(d). The diagram is actually represented as the top-view of the 7128S chip. A sample pin assignment is shown below. Note that
- VCC (VCCIO and VCCINT) and GND pins of section 6.3.
- Signals a, b, c, d and f are assigned to pins 12, 11, 10, 9 and 73 respectively.
- Few additional pins, including pins 1, 2, 83 and 84, are assigned to GND.

Device: EM7128SLC84-6

```
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75
```

- a=12 VCCIO=13 #TDO=14 #GND=15 #WDO=16 #WDE=17 #RESERVED=18
- #WDE=19 #WDE=20 #RESERVED=21 #RESERVED=22 #RESERVED=23 #RESERVED=24 #RESERVED=25
- #RESERVED=26 #GND=27 #RESERVED=28 #RESERVED=29 #RESERVED=30 #RESERVED=31 #GND=32

```
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75
```
6.8. Wire and test the device

(a) Make sure that the power of CADET is off.
(b) Connect circuit’s input and output pins to the switches and LED indicators.
(c) Turn on the power.
(d) Verify the correctness of the circuit.
(e) Construct 74LS163 test pattern generator. Verify the operation of using test pattern
    generator and logic analyzer.
(f) Remove the wires that are connected to input/output signals.

6.9. Program and test the programmable counter

(a) A simple counter was designed in section 6.2 of experiment 7. Recall that it works as a mod-
    5 counter and mod-3 counter. The counting sequence is either from 000 to 100 or from 000
to 010. The counting is determined by a selection signal sel. The counter counts 5 when sel is “0”, and counts 3 when sel is “1”. There is also one output signal, pulse, which goes high
every 5 or 3 clocks
(b) Set the design file as project and compile the project using EPM7128SLC84 device.
(c) Follow the previous procedure to program the device.
(d) Check the report file for pin assignment. The VCC and GND pins should remain the same,
    except for pin 83, which should be assigned to the clock signal now.
(e) Find the pin assignment of other signals and connect the input and output signals accordingly.
    Use manual clock and LED indicators to verify its operation.
(f) Construct 74LS163 test pattern generator. Connect Qd to sel. Verify the operation of your
    circuit using logic analyzer.
(g) Remove the wires that are connected to input/output signals.