Experiment 6
Analysis and Design of Finite State Machine

1. Purpose
To analyze and synthesize finite state machine (FSM) using SSI/MSI components.

2. Prelab
Each group member has to do his/her own work. Bring the design paper, which shows how you derive the circuit, circuit diagram printout and simulation printout to lab and let instructor/TA initial it. Attach the initialed copies to the end of your report
(a). Derive the state diagram of 6.1(a).
(b). Use Max Plus II to draw the circuit diagram of 6.1(a) and then do simulation.
(c). Design the FSM of section 6.2. Use Max Plus II to draw the circuit diagram and then do simulation.

3. Reference
Chapter 7 of Digital Design: Principles and Practice.

4. Discussion
4.1. Edge-triggered D-type Flip-Flop
D FF is the most commonly used component in sequential circuits. It is a basic memory element. In a positive-edge triggered D FF, it “samples” input (D) when the clock signal changes from low to high (i.e., rising edge) and memorizes input’s value (which appears in output Q). The value will remain unchanged until the next rising edge. When the value of an FF is set this way, its operation is known as synchronous. FF also frequently includes a reset (or clear) signal and/or a preset (set) signal to put “0” or “1” into its memory. These signals are not controlled by clock and are known as asynchronous. An important rule in modern digital design is to keep the circuit complete synchronous; i.e., do not use asynchronous signals to change FF’s state. Asynchronous signals should only be used for circuit initialization (e.g., clear all FFs to 0 when the power is turned on).

4.2. FSM Testing and Timing Diagram
To test a sequential circuit is more difficult because the outputs depend not only the inputs but also the states of internal FFs. In addition to generate input test vector, as in combinational circuit, we also need to monitor the internal state (Q outputs of FFs) and verify the state transition of FSM. The best way to represent this information is to use a timing diagram.
A simple FSM with input go and output pulse, and a sample testing timing diagram is shown below. Note that the states are encoded into by two bits (q2 and q1), and the state assignment of s1, s2, and s3 is 01, 10 and 11 respectively.

The key of the timing diagram is to show the state transition. The state is represented by q1.Q and q2.Q (as well as the symbolic ss). The FSM is reset to state s1 by reset signal initially. It then transits according to the value of input signal go and internal states. Note that transition only occurs at the rising edge of the clock. A similar timing diagram (except ss) can be observed on a logic analyzer and can be used to verify the operation of the FSM.

5. Components
74LS74 and necessary NAND/NOT/OR gates.

6. Procedures
6.1. Analysis of FSM
(a) A synchronous sequential circuit is shown below. Determine the excitation equations of D0 and D1. Derive the state diagram for this circuit.

(b). Construct the circuit using one 74LS74 and one 74LS00.
(c) Connect reset to a switch, and connect the clock to a debounced push-button switch.
   Connect Q0, Q1 and Z to LED indicators.
(d). Generate a reset pulse to set the D FFs to 00. Manually generate clocks and observe the state transition and output. Verify that the circuit operates according to the state diagram of part (a).
(e). Connect clock to 10 KHz output of function generator.
(f). Verify the operation of FSM using logic analyzer.

6.2. Synthesis of FSM

(a). An FSM circuit is specified as follows. There are three states S0, S1 and S2. There is one output, Z. Z becomes “1” when the FSM is in state S1 and becomes “0” when the FSM is in states S0 or S2. There are two inputs, F and R, which controls the direction (forward or reverse) of state transition. The state diagram is shown below:

(b). Synthesize this FSM using two D-type FFs. Derive the excitation equations and output equation.

(c). Construct the FSM using one 74LS74 and other necessary components. You can use any available TTL devices (simple gates, multiplexer, decoder etc.) to implement the next-state logic and output logic.

(d). Connect F and R to two switches and clock to a debounced push-button switch. Connect Q outputs of two FFs and Z to LED indicators.

(e). Manually generate clocks and observe the state transition and output. Flip input switches if necessary. Verify that the circuit operates according to the state diagram of part (a).

(f). Construct 74LS163 test pattern generator. Connect Qd and Qa to F and R. Observe the state transition and output and verify the operation of your circuit using logic analyzer.