Experiment 2

Design Capture and Simulation Using Altera Max Plus II Software

1. Purpose
To learn to use EDA tool to do design capture and simulation.

2. Prelab
Carefully read the experiment discussion and procedure.

3. Reference
Max Plus II Getting Started by Altera Co.

4. Discussion

4.1. Altera Max Plus II Software
Designing and implementing a digital circuit can be very involved. Computers now can provide some degree of assistance and automate part of the process. It is known as Electronic Design Automation (EDA). We are using a software package known as Max Plus II from Altera Corporation. It is a complete package to design programmable logic device based circuits and includes all key EDA software tools. The Max Plus II package consists of following elements:

1. Schematic design entry: to enter the design as a circuit diagram.
2. HDL design entry: to describe the design using HDL (Hardware Description Language).
3. Synthesis and Placement/Routing: to synthesize and optimize the circuit and covert it to fit into a programmable logic device. It is known as compiling in Max Plus II.
4. Simulation: to simulate the operation of a circuit without physical implementation.
5. Device programming: program (burn) a programmable logic device.

The first part of the course focuses on schematic entry and simulation of TTL based circuits. The second part will cover other software elements as well as programmable logic devices.

A typical design flow of TTL circuits is shown below:
In this flow, we first design our circuit and draw the schematic in computer, and then perform simulation to verify its operation. If the response is not correct, we need to revise the design and repeat the process. After the circuit is verified, we can then wire the circuit and do physical testing. Since constructing and debugging a physical circuit is a laborious, tedious and error-prone task, it is always better to do software simulation in computer first and catch error in an earlier stage.

4.2. More about Altera Max Plus II Software

Max Plus II is a real industrial-strength software package and contains many features. This experiment helps you to get started and to perform basic schematic capture and simulation. It is not comprehensive and is not a replacement for the manual. Max Plus II has a through on-line help and it is a good way to learn more about the software. After you complete the experiment procedure, play with the software, get familiar with the development environment and learn more about its menus, icon buttons etc. Consult the on-line manual if you have any doubt.

If you are interested, you can also look at the complete user guide Max Plus II Getting Started (a big 5.4 MB file, more than 300 pages), which can be can be found on line at http://www.altera.com/literature/manual/81_gs.pdf. You can also check Altera’s web site at http://www.altera.com, which is well organized and provides lots of useful information.

Since Max Plus II is real industrial-strength software, it is very expensive. However, it is possible for you to get a student version for your own PC. For our lab purpose, the student version contains most of the needed features. The software is fairly large (48 MB) and you can obtain it from Altera website. After installing the software, you need to record the serial number and contact Altera for the authorization code. The download/authorization website url is: http://www.altera.com/education/univ/univ-students.html

5. Components

Bring a blank floppy diskette to save your file.

6. Procedures

6.1. Start Max Plus II

(a). Follow the procedure provided by network administrator and log on to your account.
(b). Start MAX Plus II.
(c). Maximize MAX Plus II window.
(d). Note that there are 5 menus: Max+plus II, File, Assign, Option and Help. Max+plus II contains all Altera applications, such as Graphic Editor, Compiler etc. Help contains comprehensive on-line documentation.

Hints: The menu of Max Plus II is context sensitive, which means different application has different menu. If you cannot find a menu, you probably haven’t activated the proper application window.

6.2. Create a project file test1.gdf

(a). Select File then New... and a dialog box appears.
(b). Select Graphic Editor File. Select .gdf file extension from the drop-down list box.
(c). Click OK and a graphic editor window appears.
(d). Select File then Save As... In the pop up window, select the network drive from Drives dialog box, type test1.gdf in File Name box and then click OK.
(e). Select File then Project... then Set Project To Current File. The title bar should be updated to reflect the change.

Hints: In Max Plus II environment, you must specify a design file as your current project file
before you can invoke other processing such as compiling and simulation. The file currently being edited is not necessary the project file. You have to explicitly specify the project file, or the old project file will be compiled and simulated.

6.3. Create a graphic file test1.gdf

We like to create the circuit below:

(a). Invoke the graphic editor window if it is not active. There is an icon bar, known as the tool palette, on the left of the window. It is shown below:

Most graphic editing functions can be done by using this bar. The first icon is selection tool and the next five are different entry tools to insert text and lines. The selection tool is a “smart” tool and the other five are rarely needed. When the selection tool is used, the mouse pointer automatically changes into object selecting, line drawing or text editing pointer as needed. The next three icons are used to adjust the display scale and are zoom in button, zoom out button and fit in window button. The next icon is connection dot toggle, which is used to enter or delete a connection dot on a line intersection. The last two icons are used to turn on or off the “rubber-banding” function. When rubber-banding is on, you can move the selected symbol(s) while preserving signal connectivity.

(b) Max Plus II provides a wide variety of components. The procedure of selecting a component symbol is listed below:
- Activate selection tool button.
• In graphic editor window, choose an insertion point in empty space and double click the mouse button. A dialog box appears.

• The components are organized in different directories, known as libraries, which are shown in the Symbol Libraries box (the actual paths of these libraries may vary and depend on installation). Double click the desired library and its components will be shown in Symbol Files box. Double click the desired symbol and it will be selected and inserted into the graphic editor window.

• If you know the exact name of component you want, just type it in Symbol Name box and press OK.

(c). We are using TTL devices in the first part of our course. They can be found in ...\mf library and are represented by symbol names starting with 74. In addition to TTL devices, few primitive symbols, such as Gnd, Vcc, input stab and output stab, are also needed. They can be found in ...\prim library. Don’t use generic components, such as 2nand, 2x8mux etc., since their behaviors may not be identical to those of TTL parts.

(d). Insert one 7400 symbol (a NAND gate) using the previous procedure. Repeat it for two more times for a total of three 7400 symbols.

(e). Insert one INPUT symbol, which represents an input port of the circuit. The symbol is in ...\prim library. Repeat it 3 more times. Also, insert one OUTPUT symbol, which represents an output port of the circuit. It is also in ...\prim library.

(f). Double click and highlight the PIN_NAME of INPUT symbol. Change the name to a. Repeat the procedure and name other three INPUT symbols to b, c, and d. Apply the same procedure to OUTPUT symbol and changes its name to f.
(g) Rearrange the diagram by moving these symbols to proper places. You can move a selected symbol by holding the mouse button and dragging it. Now the diagram looks like follows:

(h) The next step is to connect the various symbols. Move the pointer to a connection point of a symbol and the pointer changes to a cross-hair (+). Press the mouse button to define the starting point of the line. Hold the button and drag the mouse to the desired end point and then release the button. You can draw either a straight line or a line with a single bend. Multiple lines are required if the connection needs two or more bends.

(i) Draw the lines to connect the symbols as follows ad complete the circuit diagram:

(j) Select File then Save to save the file.

6.4. Compile the project test1.gdf

(a) Select Max+plus II then Compiler and the compiler window appears.
(b) Click Start in Compiler window and compiler starts execution.
(c) A message window will pop up. If there is any error, go to the graphic editor, fix the problem and compile again.
   Hint: In message window, select an error and click on Locate button, Max Plus II will place the mouse pointer at the corresponding error position.

6.5. Create simulation test vector test1.scf

(a) When we simulate a circuit, we need to specify the values of input signals and examine the results of output signals and internal signals (known as buried nodes). In Max plus II, all these signals can be displayed as waveforms in waveform editor window. A representative window is shown below:
To simulate a circuit, the basic steps are:

- Choose the signals that you wish to examine.
- Specify the values of input signals, which are known as test vectors.
- Save this waveform specification as a file.
- Perform simulation using this file.
- Examine the response of internal and output signals.

The following procedure describes how to choose signals and create test vectors in waveform editor window.

(b). Select Max+plus II then Waveform Editor and the waveform editor window appears
(c). Select Node then Enter Nodes from SNF ... and a dialog window appears.
(d). Click List and a set of signal appears in the Available Nodes and Groups window.
(e). Highlight a(l) b(l) c(l) d(l) and f(O) and then click => button to move the signals to right window. Click OK. Now the selected signals appear in waveform editor window.
(f). Rearrange the signal order to a(l), b(l), c(l), d(l) and f(O) by dragging them into proper places. Adjust (zoom in/out) the display scale to shown entire 1 μ second in window.
(g). Press left mouse button and highlight signal a from 100 ns to 200 ns. Select Edit then Overwrite then High(1). Now the selected part of signal a should become 1.
(h). Repeat the previous procedure to set a b c d to be “1000” between 100 ns to 200 ns, “1100” between 200ns and 300 ns, “1010” between 300 ns and 400 ns, and “1111” between 400 ns and 500 ns.
(i). Select File then Save As .... In the pop-up window, type test1.scf in the file name entry and click OK.
(j). If you wish, try the icons on the left icon bar: they provide shortcut for editing waveform and zooming in/out timing diagram.

6.6. Simulate the project test1.gdf

(a). Select Max+plus II then Simulator and the simulator window appears. Click Start.
(b). When it is done, select Max+plus II then Waveform Editor and the output waveform of f should appear. Verify the correctness of the output waveform.

6.7. Hierarchy Display

(a). Select Max+plus II then Hierarchy Display and the hierarchy window appears. It is a handy tool that shows all the relevant information. Note that that there are several files associated with root test1. The gdf and scf are the files test1.gdf and test1.scf you just created. You can double click these files to activate the corresponding windows.
(b). Activate graphic windows. Select File then Print... and the print window appears. Click OK to print the circuit diagram.®
(c). Activate waveform windows. Print the timing diagram.®
(d). Select File then Exit Max+plus II. Click OK to close the program.
(e). If you wish have a backup copy, copy the files test1.gdf and test1.scf to your floppy diskette.
6.8. Create and simulate project test2

(a). The second circuit to be created and simulated is shown below:

74163 is used an input pattern generator to test the previous circuit. 74163 is configured in free-running mode and works as a mod 16 counter. The counting patterns of output signals Qd, Qc, Qb and Qa are 0000, 0001, 0010, 0011, ..., 1110, 1111. Note that the patterns include all possible combinations of four input signals, and thus can be used as a pattern generator to exhaustively test a circuit with 4 input signals.

(b). Create a graphic file test2.gdf and set it as the project file.

(c). Invoke the graphic editor to enter the second circuit diagram. Save the file.

(d). Compile the project.

(e). If no error, print the graphic file. ©

(f). Invoke the waveform editor and insert clk(I) and f(0).

(g). In this circuit, we also need to observe the values of test vectors; i.e., the values of Qd, Qc, Qb and Qa. They are known as the “buried nodes” since they are neither input nor output.

(h). Select Node then Enter Nodes from SNF … again. In the dialog window, check Registered in Type window (since Qd, Qc, Qb and Qa are outputs of registers) and then press List.

(i). Now Qd, Qc, Qb and Qa appear as […]p74163|sub:QD,Q(B), … , and […]p74163|sub:QA,Q(B) in the Available Nodes and Groups window. Select and insert them into the waveform editor.

(j). Rearrange the signal order to clk(I), …QD,Q(B), …QC,Q(B), …QB,Q(B), …QA,Q(B) and f(0) by dragging them into proper places.

(k). The default simulation duration is 1 μ second, which is not long enough for the second circuit. Select File then End time… and then enter 4.0us. This extends the simulation time up to 4 μ seconds.

(l). Highlight signal clk. Select Edit then Overwrite… then Clock… A dialog window appears. Click OK and the clk channel becomes a square wave with a period of 200 ns. Save the waveform file.

(m). Invoke the simulator and simulate the circuit.

(n). Invoke waveform editor again. Use the zoom function to adjust the time scale to get a better view. Verify the correctness of the output waveform.

(o). Print the timing diagram. ©

(p). Close Max Plus II program.

(q). If you wish, copy the files to your floppy diskette.

(r). Logout Windows.